CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (withdrawn): A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

at least one of said lower and upper capacitor electrodes being a conductive layer;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed between said conductive layer and said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

2 (withdrawn): The storage capacitor according to claim 1 configured to form a part of a DRAM memory cell.

3 (withdrawn): The storage capacitor according to claim 1, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

4 (withdrawn): The storage capacitor according to claim 1, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

5 (withdrawn): The storage capacitor according to claim 1, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

6 (withdrawn): The storage capacitor according to claim 1, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

7 (withdrawn): The storage capacitor according to claim 1, wherein said doped layer has a dopant distribution with a gradient.

8 (original): A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

at least one of said lower and upper capacitor electrodes being a conductive layer;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed on a side of said conductive layer remote from said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

9 (original): The storage capacitor according to claim 8 configured to form a part of a DRAM memory cell.

10 (original): The storage capacitor according to claim 8, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

11 (original): The storage capacitor according to claim 8, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

12 (original): The storage capacitor according to claim 8, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

13 (original): The storage capacitor according to claim 8, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

14 (original): The storage capacitor according to claim 8, wherein said doped layer has a dopant distribution with a gradient.

15 (withdrawn): A storage capacitor, comprising:

a conductive layer forming a lower capacitor electrode;

a storage dielectric;

an upper capacitor electrode; and

a doped Si layer disposed between said conductive layer and said storage dielectric.

16 (withdrawn): The storage capacitor according to claim 15 configured to form a part of a DRAM memory cell.

17 (withdrawn): The storage capacitor according to claim 15, wherein a dopant for said Si layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

18 (withdrawn): The storage capacitor according to claim 15, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

19 (withdrawn): The storage capacitor according to claim 15, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

20 (withdrawn): The storage capacitor according to claim 15, wherein said Si layer contains a dopant introduced with a gradient.

21 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 1 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

22 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 8 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

23 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 15 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

24 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 1 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

25 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 8 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

26 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 15 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

27 (withdrawn): A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

at least one of said lower and upper capacitor electrodes being a conductive filling;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer disposed between said conductive filling and said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

28 (withdrawn): The storage capacitor according to claim 27 configured to form a part of a DRAM memory cell.

29 (withdrawn): The storage capacitor according to claim 27, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

30 (withdrawn): The storage capacitor according to claim 27, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

31 (withdrawn): The storage capacitor according to claim 27, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

32 (withdrawn): The storage capacitor according to claim 27, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

33 (withdrawn): The storage capacitor according to claim 27, wherein said doped layer has a dopant distribution with a gradient.

34 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 27 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

35 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 27 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.